

## Final Report Summary

# Development of a Passive Filter Design Methodology for Powerline Applications



**Gigle Semiconductor**  
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Gigle Semiconductor is engaged in the development of novel integrated circuits for the powerline market which will facilitate the distribution of multimedia in homes over the existing power cables. Gigle's innovative techniques are capable of providing the necessary very high data rates whilst adapting dynamically to the varying line conditions of a typical house mains network. Regulatory requirements place strict limits on the out of band emissions from such equipment, and the various antialiasing and smoothing functions require filtering which is unsuited to implementation on an integrated circuit.

A natural part of integrated circuit design is to develop applications circuits which users can treat as reference designs for their equipment. As such they require to meet demanding filter profiles over the normal distributions of commercially available components, with the least number and cost of components and to fit into a specific, small physical volume. Gigle need to develop such circuits and to demonstrate that their products are capable of gaining regulatory approval when so implemented.

### Project Aims

Gigle's choice of ISLI as its TTOM partner was motivated by ISLI's wide experience of EDA tools and techniques, its analog design expertise and its experience in system level decisions. The opportunities for longer-term collaborations were an important consideration. The aims of the project were to perform:

- An investigation into the available tools for filter design methodology.
- An analysis of the kinds of filter suited cost-effectively to Gigle's application.
- Actual design of some prototype filters to Gigle's system specifications.

### Project Outcomes

ISLI's expertise has enabled Gigle Semiconductor to rapidly advance their understanding of discrete passive filter design and limitations with a view to developing cost-effective applications circuits for their range of powerline integrated circuits. Suitable tools were identified to facilitate rapid design of passive filters to demanding specifications, and the tradeoffs of the costs and performance of alternative filter architectures were successfully explored. In addition it was possible to explore the effects of component tolerancing and parasitics in a fast-turn environment.

A number of actual filter designs to various specifications were produced as part of this project and these will be implemented in pcb form to verify the correspondence between simulated and real-world performance using non-ideal components. A longer-term extension to the project is envisaged to refine the methodologies and to enable the amalgamation of the filter design into the overall integrated circuit design flow.

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